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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,287	07/23/2003	Jung Kook Park	CU-3301	7895

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
11/09/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto.actions@wwplaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/625,287	PARK ET AL.	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 10* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama (US 20030179173 A1).

Regarding **Claim 1**, Koyama teaches an impulsive type liquid crystal driving device (Koyama, Figs. 2 and 3), comprising:

a liquid crystal panel comprising:

a plurality of gate bus lines arranged in a first direction (Koyama, Fig. 3 Gy); and

a plurality of data bus lines arranged in a second direction substantially perpendicular to the first direction (Koyama, Fig. 3 Sx);

a gate driver section for sequentially scanning the plurality of gate bus lines during and active address interval in response to a vertical starting signal, a vertical clock signal (Koyama, Fig. 14 GSP GCL GCLB), and an output enable signal and for

scanning the plurality of gate bus lines during a vertical blanking interval in a unit of a predetermined number of lines (Koyama, Fig. 14 ENB); and

a current boosting section for increasing current amount supplied to the gate bus lines during the vertical blanking interval in response to a pulse width modulation signal (Koyama, paragraphs [0028 and 0065] Figs. 16A and 16B).

Regarding **Claim 3**, Koyama further teaches wherein the gate driver section comprises a plurality of gate driver integrated circuits for scanning the plurality of gate bus lines in response to the second vertical starting signal, the vertical clock signal, and the output enable signal (Koyama, Fig. 14 GSP GCL and GCLB all gate driver ICs respond to both GCL and GCLB; and each shift register passes a "new" start signal to the next shift register by shifting it down to the next stage).

Regarding **Claim 4**, Koyama further teaches wherein each of the gate driver integrated circuit comprises:

a shift register section which sequentially shifts the vertical starting signal and outputs the shifted vertical starting signal during the active address interval (Koyama, Fig. 14 GSP is actively pushed down the shift register using GCL and GCLB), and which generates a predetermined number of first output signals at substantially the same time the shifted vertical starting signal is outputted after receiving the vertical starting signal during the vertical blanking interval, in response to the vertical clock signal and the output signal (Koyama, Fig. 14 outputs to the NAND gates 3607 in sync w/ the clocks and the start pulses, blanking occurs in sync w/ gate signals as well, Figs. 16A and 16B);

a second shift register section which receives the signal shifted by the first shift register section, sequentially shift the received signal, and then outputs shifted received signal during the active address interval, and which generates a predetermined number of second output signals at substantially the same time the shifted received signal is outputted after receiving the signal shifted by the first shift register section during the vertical blanking interval, in response to the vertical clock signal (Koyama, Fig. 14 first and second half the shift registers can be considered distinct from one another but they perform similar function although the second half receives its start pulse from the last stage of the first half);

a plurality of level shifters which level-convert the output signals of the first and second shift register section (Koyama, Fig 14 paragraph [0094]); and

a plurality of buffer amplifiers which amplify the signals converted by the plurality of level shifters and then generates gate on/off signals (Koyama, Fig 14 paragraph [0094]).

Regarding **Claim 5**, Koyama further teaches wherein the first shift register section (Koyama, Fig. 14 first half of shift register) comprises:

a predetermined number of first switches which selection either the vertical starting signal or an internally shifted signal in response to the output enable signal (Koyama, Fig. 14 NOR gates select either the start signal or the shifted signal output from the shift registers which is a copy of the start signal just delayed according to the output enable); and

a predetermined number of first shift registers which receive the vertical starting signal and then output it after sequentially shifting it, when the internally shifted signal is selected (Koyama, Fig. 14 shift registers shift the start signal sequentially down the shift register one by one according to GCL and GCLB), and which receive the vertical starting signal and then output the predetermined number of first output signals at the same time without shifting, when the vertical starting signal is selected (Koyama, Fig. 14 when the vertical start signal is selected and the enable is selected all outputs are output simultaneously, Fig. 16B non-display period the whole screen turns dark).

Regarding **Claim 6**, Koyama further teaches wherein the second shift register section (Koyama, Fig. 14 first half of shift register) includes:

a plurality of second switches which select either the signal shifted by the first register section or an internally shifted signal in response to the output enable signal (Koyama, Fig. 14 NOR gates select either the start signal or the shifted signal output from the shift registers which is a copy of the start signal just delayed according to the output enable); and

a predetermined number of second shift registers which receive the vertical starting signal and then output it after sequentially shifting it, when the internally shifted signal is selected, and which receive the shifted signal and then output the predetermined number of second output signals at the same time without shift, when the signal shifted by the first shift register section is selected (Koyama, Fig. 14 second half of shift register has same operation as first half only the start signal comes from the last stage of the first half instead of the original start signal GSP).

Regarding **Claim 7**, wherein the current boosting section includes a plurality of current booster circuit for receiving a plurality of gate on/off signals outputted from the gate driver section and a pulse width modulation signal, respectively (Koyama, Fig. 14 shift register is inherently a current booster for the fact that if the pulse width increases the current to the gate line increases because of the increase duty paragraph [0028 and 0065] Fig. 16A and 16B).

Regarding **Claim 10**, Koyama further teaches wherein the current amount generating in the current boosting section is adjusted according to a duty ratio of the pulse width modulation signal (Koyama, Fig. 14 current adjustment is proportional to duty of pulse width modulation signal [0028 and 0065] Fig. 16A and 16B).

Response to Arguments

Applicant's arguments with respect to claims 1, 3-7 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claims 8 and 9 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art fails to teach "wherein the current booster circuit that includes:

an operational amplifier having a non-inverting terminal and an inverting terminal;

a first resistor coupled between the non-inverting terminal and a ground;

a first capacitor coupled in parallel to the first resistor;

a second capacitor coupled between a first input terminal and the ground;

a second resistor of which one end is coupled to the first input terminal;

a first bipolar transistor coupled between the other end of the second resistor and a ground, and turned on according to an output signal of the operational amplifier; a third resistor of which one end is coupled to the first input terminal;

a second bipolar transistor coupled between other end of the third resistor and the non-inverting terminal, and turned on according to an output signal of other end of the second resistor;

a fourth resistor coupled between the first input terminal and the non-inverting terminal;

a third capacitor coupled between the inverting terminal of the operational amplifier and an output terminal;

a fifth resistor coupled between a second input terminal and the inverting terminal;

a sixth resistor coupled between the inverting terminal and a ground; and

a fourth capacitor coupled in parallel to the sixth resistor", *wherein the current booster is specifically used for the gate driver.*

Emphasis added.

Claim 9 depends from claim 8 and are allowed for at least the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ke Xiao/
Examiner, Art Unit 2629